Q1 T_2 during the logic one state of the CLK signal, the cell 12 begins furnishing the bit 52 to the cell 14a, as depicted in Fig. 3. The cells 14a and 14b then relay the bits 50 and 52 in a time multiplexed fashion.

Please replace the paragraph beginning on line 25 of page 3 with the following:

Q2 Fig. 3 depicts waveforms illustrating signals of the double pumped bus system of Fig. 2.

Please replace the paragraph beginning on line 27 of page 3 with the following:

Q3 Figs. 4 and 6 are schematic diagrams of double pumped bus cells according to embodiments of the invention.

Please replace the paragraph beginning on line 29 of page 3 with the following:

Q4 Fig. 5 is a more detailed schematic diagram of the cell of Fig. 4 according to an embodiment of the invention.

Please replace the paragraph beginning on line 1 of page 4 with the following:

Q5 Fig. 7 is a schematic diagram of a double pumped bus cell system according to an embodiment of the invention.

Please replace the paragraph beginning on line 3 of page 4 with the following:

Q6 Fig. 8 is a schematic diagram of a computer system according to an embodiment of the invention.

Please replace the paragraph beginning on line 7 of page 4 with the following:

Q7 Referring to Fig. 4, an embodiment 100 of a double pumped bus cell in accordance with the invention may be set up to communicate either one or two sets of data. More specifically, in some embodiments of the invention, an EN signal that is received by the cell 100 may be asserted (driven high, for example) to enable the cell 100 to latch, store and retransmit bits of data from two different data sets in a time multiplexed fashion. In this manner, a data line 107 communicates a signal (called DATAIN) that indicates bits of data from a first data set and a second data set. The bits of the first data set are interleaved, or alternate, in time with the bits of the second data set.

Please replace the paragraph beginning on line 25 of page 5 with the following:

To accomplish the above-described features, in some embodiments of the invention, the cell 100 may include logic, such as an AND gate 112, that receives the CLK and EN signals. The output terminal of the AND gate 112 is coupled to the inverting clock input terminal of the bit latch 104, and the clock input terminal of the bit latch 102 receives the CLK signal. Because the bit latches 102 and 104, in some embodiments of the invention, invert the logic levels of the stored bits, the cell 100 may include an inverter 108 that is coupled between the data input line 107 and the input terminals of the bit latches 102 and 104. When the EN signal is de-asserted, the output terminal of the AND gate 112 is de-asserted, regardless of the logic level of the CLK signal, and thus, the bit latch 104 does not store any new data as long as the EN signal remains de-asserted. However, when the EN signal is asserted, the CLK signal controls the signal at the output terminal of the AND gate 112 and thus, controls the reception of data into the bit latch 104.

Please replace the paragraph beginning on line 6 of page 6 with the following:

Fig. 5 depicts a more detailed schematic diagram of the cell 100 in accordance with some embodiments of the invention. As shown, the bit latch 102 may include a circuit 140 that is effectively a complementary metal oxide semiconductor (CMOS) inverter that is enabled when the CLK signal (that alternates between logic one and logic zero states) is in a logic one state to latch the bit that is indicated by the DATAIN signal. To accomplish this, the circuit 140 includes an n-channel metal-oxide-semiconductor field-effect-transistor (NMOSFET) 148 that has its source terminal coupled to ground and its drain terminal coupled to the source terminal of another NMOSFET 146. The drain terminal of the NMOSFET 146 is coupled to the drain terminal of a p-channel metal-oxide-semiconductor field-effect-transistor (PMOSFET) 144. The source terminal of the PMOSFET 144 is coupled to the drain terminal of another PMOSFET 142, and the drain terminal of the PMOSFET 142 is coupled to a positive voltage supply level (called V_{DD}). The gate terminals of the PMOSFET 144 and the NMOSFET 146 respond to the logical state of the CLK signal to control when the circuit 140 is enabled. In this manner, the gate terminal of the PMOSFET 144 is coupled to a clock input terminal 131 (that furnishes the CLK signal) via a chain 124 of three serially coupled inverters 240 that invert the CLK signal to receive an inverted version of the CLK signal. The gate terminal of the NMOSFET 146 is

coupled to a chain 123 of serially coupled inverters 120 to the clock line 131 to receive an indication of the CLK signal. The gate terminals of the PMOSFET 142 and the NMOSFET 148 are coupled to the data input line 107.

Please replace the paragraph beginning on line 5 of page 7 with the following:

Similar to the bit latch 102, the bit latch 104 includes the circuit 140 and the bit latch that is formed from inverters 160 and 162. However, unlike the bit latch 102, the gate terminals of the circuit 140 of the bit latch 104 are connected differently. In this manner, the gate terminal of the PMOSFET 144 is coupled to the output terminal of a NAND gate 124, and the gate terminal of the NMOSFET 146 is coupled to the output terminal of an inverter 136 that has its input terminal coupled to the output terminal of the NAND gate 124. One input terminal of the NAND gate 124 is coupled between the inverter 120 to receive an inverted indication of the CLK signal, and the other input terminal of the NAND gate 124 is coupled to an enable input line 113 to receive the EN signal. Thus, when the EN signal is asserted, the circuit 140 of the bit latch 104 is enabled during the logic zero state of the CLK signal to update the bit that is stored by the inverters 160 and 162 of the circuit 104. During the logic one state of the CLK signal and when the EN signal is de-asserted, the circuit 140 is disabled. Thus, when the CLK signal transitions from the logic zero to the logic one state on a positive edge, the CMOS inverter becomes disabled to latch the bit that is stored in the inverters 160 and 162 of the bit latch 104.

Please replace the paragraph beginning on line 20 of page 7 with the following:

In some embodiments of the invention, the multiplexer 106 includes two CMOS pass gates 172 and 174. The input terminal of the CMOS pass gate 172 is coupled to the output terminal of the inverter 164 of the bit latch 102, and the output terminal of the CMOS pass gate 172 is coupled to a node 168 that forms the output terminal of the multiplexer 106. The inverting control, or selection, terminal of the pass gate 172 is coupled to the gate terminal of the NMOSFET 146 of the bit latch 102, and the non-inverting control, or selection, terminal of the pass gate 172 is coupled to the gate terminal of the PMOSFET 144 of the bit latch 102. Thus, due to this arrangement, the output terminal of the bit latch 102 is coupled to the output terminal of the multiplexer 106 when the CLK signal has a logic zero level. The input terminal of the CMOS pass gate 174 is coupled to the output terminal of the inverter 164 of the bit latch 104,

and the output terminal of the CMOS pass gate 174 is coupled to the node 168. The inverting control terminal of the pass gate 174 is coupled to the non-inverting control terminal of the pass gate 172, and the non-inverting control terminal of the pass gate 174 is coupled to the inverting control terminal of the pass gate 172. Thus, due to this arrangement, the output terminal of the bit latch 104 is coupled to the output terminal of the multiplexer 106 when the CLK signal has a logic one level. In some embodiments of the invention, the inverter 110 may include a chain of three inverters 109 that are coupled between the node 168 and the output terminal 170.

Please replace the paragraph beginning on line 7 of page 8 with the following:

The cell 100 that is described above receives time-multiplexed bits of data from a single wire. However, in some embodiments of the invention, a cell 200 that is depicted in Fig. 6 may be used in place of the cell 100. The cell 200 has a similar design to the cell 100 except for the following features. Unlike the cell 100, the cell 200 has two data input lines 203 and 205 (instead of one) to receive bits of data from circuits that are associated with two different data sets. In this manner, the inverter 108 (see Fig. 4) of the cell 100 is replaced by two inverters 202 and 207 of the circuit 200. The input terminal of the inverter 202 receives a signal (called DATA1) that is indicative of bits of data from the first data set, and the input terminal of the inverter 207 receives a signal (called DATA2) that is indicative of bits of data from the second data set. The output terminal of the inverter 202 is coupled to the data input line of the bit latch 102, and the output terminal of the inverter 207 is coupled to the data input line of the bit latch 104.

Please replace the paragraph beginning on line 19 of page 8 with the following:

Referring to Fig. 7, in some embodiments of the invention, the cells 100 (the enabled cells 100a and the disabled cells 100b, as described below) and 200 may be used to form a double pumped bus chain 220 for purposes of communicating the bits of data from the first and second data sets across an integrated circuit, for example. In this manner, the cell 200 is the first in the chain 220 to arrange bits from the two different data sets in a time interleaved fashion. The cells 100 may be serially coupled together after the cell 200. As shown, to disable the flow of the bits of the data set that is associated with the DATA2 signal, every other cell 100 is disabled, as depicted in Fig. 7 by the enabled cells 100a and the disabled cells 100b. This alternative